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| EXAMINER | |
|---|---|
| KIM, HONG CHONG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | 5 |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/938,782 | KEAYS, BRADY L. | |
| | Examiner | Art Unit | |
| | Hong C Kim | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12 and 14-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

**Detailed Action**

1. Claims 1-12, and 14-51 are presented for examination. This office action is in response to the amendment filed on 1/15/04.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 33-38, 4, 5, 9-12, 14, 15-16, 19, 20, 23-25, 26-29, 32, 42-46 and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Itoh et al. (Itoh) U.S. Patent 5,966,720.

As to claim 33 , Itoh discloses the invention as claimed. Itoh discloses a method of operating a Flash memory device (Fig. 3) comprising: storing an erase block management data structure (Fig. 3 Ref. 11) in each erase block of a plurality of erase blocks (Fig. 3 B0- Bm) of a flash memory array (Fig. 3), wherein each erase block contains a plurality of sectors (Fig. 3 Sectors 00- mm) and the erase block management data structure of each erase block is stored in a plurality of control data sections (Fig. 3 Refs. 10, 11 and 13) of a subset of the plurality of sectors (Fig. 3).

As to claim 34, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein storing the erase block management data structure further comprises storing the erase block management data structure in an erase block management data field of each control data section of the subset of sectors (Fig. 3).

As to claim 35, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein storing the erase block management data structure in an erase block management data field of each control data section of the subset of sectors further comprises storing an erase block management data value in a control data section of the subset of sectors (Fig. 3).

As to claim 36, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein storing the erase block management data structure in an erase block management data field of each control data section of the subset of sectors further comprises storing an erase block management data value in a 6 byte data field (col. 4 lines 20-28) of each control data section of the subset of sectors (Fig. 3).

As to claim 37, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein storing the erase block management data structure further comprises storing a plurality of differing erase block management data in the control data sections of the subset of sectors of each erase block (Fig. 3).

As to claim 38, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein storing the erase block management data structure in a subset of the plurality of sectors of each erase block further comprises storing the erase block management data structure in the control data sections of an initial 6 sectors of the erase block (Fig. 3).

As to claim 4 , Itoh discloses the invention as claimed. Itoh discloses a Flash memory device (Fig. 3) comprising: a memory array containing a plurality of floating gate memory cells (Fig. 3 and flash memory reads on this limitation) arranged in a plurality of erase blocks (Fig. 3 B0 -Bm), wherein each of the plurality of erase blocks is further divided into a plurality of sectors (Fig. 3 sector 00 – mm), each sector of the plurality of sectors having a user data section (Fig. 3 Ref. 12) and a control data section (Fig. 3 Ref 11); and an erase block management data structure (Fig. 3 Ref. 11) arranged in the control data sections of a subset of sectors each erase block of the plurality of erase blocks (Fig. 3) .

As to claim 5, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the control data sections of the subset of sectors contain a plurality of differing erase block management data fields (Fig. 3).

As to claim 9 , Itoh discloses the invention as claimed. Itoh discloses a Flash memory device comprising: a memory array (Fig. 3) containing a plurality of floating

gate memory cells (Fig. 3 and flash memory reads on this limitation) divided into a plurality of erase blocks (Fig. 3 B0-Bm), wherein each of the plurality of erase blocks is further divided into a plurality of sectors (Fig. 3 sector 00 – mm), each sector of the plurality of sectors having a user data section (Fig. 3 Ref. 12) and a control data section (Fig. 3 Ref 11); and an erase block management data structure (Fig. 3 Ref. 11) arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks (Fig. 3).

As to claim 10, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the control data section of each sector of the first set of sectors has an erase block management data field (Fig. 3).

As to claim 11, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the erase block management data fields of the first set of sectors contain a plurality of differing the erase block management data (Fig. 3).

As to claim 12, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the erase block management data field is a six byte data field (Fig. 3 and col. 4 lines 20-28).

As to claim 14, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the first set of sectors of the plurality of sectors comprises a first six sectors of each erase block of the plurality of erase blocks (Fig. 3).

As to claim 32 , Itoh discloses the invention as claimed. Itoh discloses a method of making a Flash memory device comprising: forming a memory array containing a plurality of floating gate memory cells (Fig. 3 and Flash memory reads on this limitation) arranged in a plurality of erase blocks (Fig. 3 b0 - bm), wherein each of the plurality of erase blocks is further divided into a plurality of sectors (Fig. 3 sector 00 – mm), each sector of the plurality of sectors having a user data section (Fig. 3 Ref. 12) and a control data section (Fig. 3 Ref 11); and forming an erase block management data structure (Fig. 3 Ref. 11) in the control data sections of a subset of sectors of each erase block of the plurality of erase blocks (Fig. 3).

As to claim 15 , Itoh discloses the invention as claimed. Itoh discloses a Flash memory device comprising: a memory array containing a plurality of floating gate memory cells (Flash memory reads on this limitation) arranged in a plurality of erase blocks (Fig. 3 B0-Bm), wherein each of the plurality of erase blocks is further divided into a plurality of sectors (Fig. 3 sector 00 – mm), each sector of the plurality of sectors having a user data section (Fig. 3 Ref. 12) and a control data section (Fig. 3 Ref 11); and an erase block management data structure (Fig. 3 Ref. 11) arranged in the control data sections of a first set of sectors each erase block of the plurality of erase blocks

(Fig. 3), wherein each erase block of the plurality of erase blocks has an erase block state (Fig. 3 Ref. 11 col. 2 lines 62-65) that is recorded in the erase block management data structure of the erase block (Fig. 3).

As to claim 16, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the erase block state is one of "erased", "invalid", "partially filled", or "fully valid" (Fig. 3 Ref. 11 col. 2 lines 62-65).

As to claim 18, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein each erase block of the plurality of erase blocks contains a contiguous range of logical sector addresses (Fig. 3).

As to claim 19, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein each erase block of the plurality of erase blocks contains a single logical sector address that is repeated within the erase block (Fig.3).

As to claim 20 , Itoh discloses the invention as claimed. Itoh discloses a Flash memory device comprising: a memory array containing a plurality of floating gate memory cells (Flash memory reads on this limitation) arranged in a plurality of erase blocks (Fig. 3 B0-Bm) wherein each of the plurality of erase blocks is further divided into a plurality of sectors (Fig. 3 sectors 00 – mm), each sector of the plurality of sectors having a user data section (Fig. 3 Ref. 12) and a control data section (Fig. 3 Ref 11); a

control circuit; and an erase block management data structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks (Fig. 3).

As to claim 23, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the control circuit manages a state of each erase block and erase block management data structure of the plurality of erase blocks (Fig. 3).

As to claim 24, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the erase block management data structure of each individual erase block of the plurality of erase blocks contains erase block management data for the individual erase block (Fig. 3).

As to claim 25, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein each erase block and erase block management data structure of the plurality of erase blocks is written with an updated user data and an updated erase block management data with a single erase block write operation (col. 2 line 62 thru col. 3 line 3).

As to claim 42 , Itoh discloses the invention as claimed. Itoh discloses a method of operating a Flash memory device comprising: placing an erase block management data structure (Fig. 3 Ref. 11) in a control data section (Fig. Refs 10, 11, 13) of a subset

of sectors of a plurality of sectors (Fig. 3 sectors 00-mm) of each erase block of a plurality of erase blocks (Fig. 3 B0 - Bm) of a Flash memory array (Fig. 3); and recording an erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks (Fig. 3 col. 2 lines 62-65).

As to claim 43, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein recording the erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks further comprises recording an erase block identifier that identifies erase block format and content in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks (Fig. 3).

As to claim 44, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein recording the erase block identifier further comprises recording an erase block identifier that identifies the erase block as containing a contiguous range of logical sector addresses (Fig. 3).

As to claim 45, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein recording the erase block identifier further comprises recording an

erase block identifier that identifies the erase block as containing a single logical sector address that is repeated within the erase block (Fig. 3).

As to claim 46, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording the erase block state as one of "erased", "invalid", "partially filled", or "fully valid" (col.2 lines 62-65).

As to claim 48, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein recording the erase block state in the erase block management data structure in the control data section of the subset of sectors of each erase block of the plurality of erase blocks further comprises recording the erase block state with an erase block operation that writes both a user data and the erase block management data in a single write operation (Fig. 3 col. 2 line 62 thru col. 3 line 3).

As to claim 26 , Itoh discloses the invention as claimed. Itoh discloses a system comprising: a host coupled to a Flash memory device (Fig. 1), wherein the Flash memory device comprises, a memory array containing a plurality of floating gate memory cells (Fig. 3 and Flash memory reads on this limitation) arranged in a plurality of erase blocks (Fig. 3 Bo- Bm), wherein each of the plurality of erase blocks is further divided into a plurality of sectors (Fig. 3 sectors 00 – mm), each sector of the plurality of

sectors having a user data section (Fig. 3 Ref. 12) and a control data section (Fig. 3 Ref 11); a control circuit; and an erase block management data (Fig. 3 Ref. 11) structure arranged in the control data sections of a first set of sectors of each erase block of the plurality of erase blocks (Fig. 3)

As to claim 27, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the Flash memory device appears to the host as a rewriteable storage device (Fig.3 and flash reads on this limitation).

As to claim 28, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the host is a processor (Fig. 2 col. 3 lines 65+) .

As to claim 29, Itoh discloses the invention as claimed in the above. Itoh further discloses wherein the host is a computer system (Fig. 2 col. 3 lines 65+).

3. Claim 33, 4, 9, 15, 20, 26, 32, and 42 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA).

As to claim 33, 4, 9, 15, 20, 26, 32, and 42 , AAPA discloses the invention as claimed. AAPA discloses a method of operating a Flash memory device (Fig. 1 Ref. 112) comprising: storing an erase block management data structure (Fig. 1 Ref. 122) in each erase block of a plurality of erase blocks (Fig. 1 Refs. 120) of a flash memory array containing a plurality of floating gate memory cells (Fig. 1 and flash memory

reads on this limitation) arranged in the plurality of erase blocks, wherein each erase block contains a plurality of sectors (Fig. 1 Ref. 116) and the erase block management data structure of each erase block is stored in a plurality of control data sections (Fig. 1 Ref. 122) of a subset of the plurality of sectors (Fig. 1).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 39, 41, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (Itoh) U.S. Patent 5,966,720 in view of Reasoner et al. (Reasoner) U.S. Patent 5,608,684.

As to claim 39 , Itoh discloses a method of operating a Flash memory device comprising: storing an erase block management data structure in a plurality of sectors (Fig. 3 Sectors 00- mm) of each erase block of a plurality of erase blocks (Fig. 3 B0 - Bm) of a Flash memory array (Fig. 3), wherein each erase block contains a plurality of sectors (Fig. 3 Sectors 00- mm) and the erase block management data structure of each erase block is stored in a plurality of control data sections of a subset of the plurality of sectors (Fig. 3). However, Itoh does not specifically disclose a fault tolerant erase block.

Reasoner discloses a fault tolerant erase block (abstract, Fig. 1 ) for the purpose of increasing reliability thereby preventing a system slow down and crash.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a fault tolerant erase block of Reasoner into the invention of Itoh for the advantages stated above.

As to claim 41, Itoh discloses the invention as claimed in the above. Reasoner further discloses wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a copy of an erase block management data field contained in a first control data section of the erase block in a second control data section of the erase block (Fig. 1, abstract).

As to claim 6, Itoh and Reasoner disclose the invention as claimed in the above. Reasoner further discloses wherein the erase block management data structure is configured in a fault tolerant data structure (Fig. 1 and abstract).

As to claim 8, Itoh and Reasoner disclose the invention as claimed in the above. Reasoner further discloses wherein the fault tolerant data structure is a copy in a second sector of the erase block of an erase block management data field contained in a first sector of the erase block (Fig. 1 and abstract).

5. Claims 40 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over as being unpatentable over Itoh et al. (Itoh) U.S. Patent 5,966,720 in view of Reasoner et al. (Reasoner) U.S. Patent 5,608,684 and further in view of Duke U.S. Patent 3,576,982.

As to claim 40, Itoh and Reasoner disclose the invention as claimed above. Reasoner further discloses wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a component of the erase block management data structure in a first erase block management data field of a first control data section (Fig. 1 and abstract), however, neither Itoh nor Reasoner specifically discloses a 1s complement copy of the component of the erase block management data structure in a second erase block management data field. However, it is well known in the memory art to using a 1s complement copy of the component of the erase block management data structure in a second erase block management data field for the purpose of saving backup data thereby increasing data reliability. For example, Duke discloses a 1s complement copy of the component of the erase block management data structure in a second erase block management data field (abstract).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a 1s complement copy of the component of the erase block management data structure in a second erase block management data field of Duke into the combined invention of Itoh and Reasoner for the advantages stated above.

As to claim 7, Itoh, Reasoner, and Duke disclose the invention as claimed in the above. Reasoner further discloses wherein the fault tolerant data structure (Fig. 1) is an erase block management data field and Duke further discloses a 1s complement copy of the erase block management data field (abstract).

6. Claims 22, 21, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (Itoh) U.S. Patent 5,923,827 in view of Applicant's Admitted Prior Art (AAPA).

As to claim 22, Itoh discloses the invention as claimed above. However, Itoh does not specifically disclose the control circuit maps a logical address to a physical address of the plurality of erase blocks. AAPA discloses the control circuit maps a logical address to a physical address of the plurality of erase blocks (block 9) for the purpose of providing virtual mapping thereby a system addressing space appears bigger and uniform than it is.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the control circuit maps a logical address to a physical address of the plurality of erase blocks of AAPA into the invention of Itoh for the advantages stated above.

As to claim 21, Itoh and AAPA disclose the invention as claimed in the above. AAPA further discloses wherein the control circuit stores equivalents of the erase block

management data structures of each erase block of the plurality of erase blocks into a RAM data structure (Fig. 1).

As to claim 49, Itoh and AAPA disclose the invention as claimed in the above. AAPA further discloses comprising storing the contents of the erase block management data structures of each erase block of the plurality of erase blocks into a RAM data structure (Fig. 1).

7. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Itoh et al. (Itoh) U.S. Patent 5,923,827.

As to claim 1, AAPA discloses a Flash memory device (Fig. 1) comprising: a control circuit(fig. 1 Ref. 110); a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks (page 2 block 4 Fig. 1 Ref. 122), wherein each erase block of the plurality of erase blocks contains 128 sectors (page 4 block 11 bottom), and each sector contains a user data section of 512 bytes (page 4 block 11 center) and control section (Fig. 1 Section 122); and a plurality of RAM control registers (Fig. 1 Ref. 114). However, AAPA does not specifically disclose an erase block management data structure formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field, wherein the 6 byte erase block management data fields of the first six sectors contain a plurality of differing erase block . Itoh discloses an erase block management data structure

formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field (Fig. 3 and col. 4 lines 20-28) for the purpose of enabling high speed processing .

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an erase block management data structure formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field of Itoh into the invention of AAPA for the advantages stated above.

As to claim 3, AAPA and Itoh disclose the invention as claimed in the above. Itoh further discloses wherein the first six sectors of each erase block of the plurality of erase blocks are arranged into 3 groups of 2 sector pairs, wherein both sectors of each 2 sector pair contains a complete copy of a erase block management data stored in the 2 sector pair (Fig. 3 and col. 4 lines 20-28).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Itoh et al. (Itoh) U.S. Patent 5,923,827 and further in view of Duke U.S. Patent 3,576,982.

As to claim 2, AAPA and Itoh disclose the invention as claimed above. However, neither AAPA nor Itoh specifically disclose erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes. Duke discloses erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes (abstract) for the purpose of saving backup data thereby increasing data reliability.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes of Duke into the combined invention of AAPA and Itoh for the advantages stated above.

9. Claims 50-51, 30-31, 17, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (Itoh) U.S. Patent 5,923,827 in view of Applicant's Admitted Prior Art (AAPA).

As to claim 50, Itoh discloses the invention as claimed above. However, Itoh does not specifically disclose the control circuit maps a logical address to a physical address of the plurality of erase blocks. AAPA discloses the control circuit maps a logical address to a physical address of the plurality of erase blocks (block 9) for the purpose of providing virtual mapping thereby a system addressing space appears bigger and uniform than it is.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the control circuit maps a logical address to a physical address of the plurality of erase blocks of AAPA into the invention of Itoh for the advantages stated above.

As to claim 51, Itoh and AAPA disclose the invention as claimed above. Itoh further discloses managing a state of each erase block and erase block management data structure (Fig. 3).

As to claim 30, Itoh and AAPA disclose the invention as claimed in the above. AAPA further discloses wherein an interface to the Flash memory device is compatible with a mass storage device (block 6).

As to claim 31, Itoh and AAPA disclose the invention as claimed in the above. AAPA further discloses wherein an interface to the Flash memory device is a PCMCIA-ATA compatible interface (block 7).

As to claims 17 and 47 Itoh and AAPA disclose the invention as claimed in the above. AAPA further further discloses wherein the erase block state is allowed to transition directly from the "partially filled" state to the "invalid" state (block 9, erasing partially filled block reads on this limitation).

***Response to Arguments***

10. Applicant's arguments filed on 1/15/04 have been fully considered but they are not persuasive. Applicant's remarks that the references not teaching a flash memory that has an erase block management data structure in the control data sections of a subset of sectors of each erase block is not considered persuasive.
Itoh discloses a flash memory that has an erase block management data structure in the control data sections of a subset of sectors of each erase block (Fig. 3).

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

12. a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

14. When responding to the office action, Applicants are advised to provide the

examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

16. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

**or faxed to TC-2100:**
(703) 872-9306

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
March 26, 2004